

Hall Ticket Number:

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Code No. : 15644 S N/O

VASAVI COLLEGE OF ENGINEERING (AUTONOMOUS), HYDERABAD
Accredited by NAAC with A++ Grade

B.E. (I.T.) V-Semester Supplementary Examinations, June-2023

Microprocessors and Interfacing

Time: 3 hours

Max. Marks: 60

Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B**

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Determine the number of bytes in the instructions: i) DCR C ii) ADI F5H	2	1	1	1
2.	Explain the function of the signals ALE and IO/M' in 8085.	2	1	1	1
3.	Explain the function of the signals DT/R' and DEN in 8086.	2	1	2	1
4.	Is the instruction MOV DS, 5000H a valid instruction, justify your answer?	2	1	2	1
5.	Explain the function of CNTL/STB in 8279.	2	1	3	1
6.	List the different modes of 8255.	2	1	3	1
7.	Explain the function of CAS0:CAS2 pins of 8259A.	2	2	4	1
8.	List the operating modes of 8253.	2	1	4	1
9.	Explain the function of TxRDY and Rx RDY pins of 8251.	2	2	5	1
10.	Give the functionality of the signal HRQ and HLDA in 8257.	2	1	5	1
Part-B (5 × 8 = 40 Marks)					
11. a)	Write an assembly language program using 8085 to a. clear the accumulator b. add 47H (use ADI instruction) c. subtract 92 H d. add 64 H e. display the results after subtracting 92H and after adding 64H at two different output ports with addresses 01H and 02H respectively. Specify the answers you would expect at the output ports.	4	3	1	2
b)	Explain with a neat diagram the architecture of 8085 processor.	4	2	1	1

Contd... 2

12. a)	Explain the different addressing modes of 8086 with suitable examples.	4	3	2	1
b)	Write an assembly language program using 8086, using assembler directives, wherever required, to count the number of positive and negative numbers from a given series of 16 bit hexa decimal numbers.	4	3	2	2
13. a)	Illustrate using the control word format how you can configure 8255 to operate the different modes of operation in I/O mode of operation.	4	3	3	2
b)	Draw timing diagrams and discuss in brief the different modes of operation of 8253 (Programmable interval timer).	4	3	3	2
14. a)	Draw and discuss the architecture of 8253 programmable interval timer.	4	2	4	1
b)	Indicate the steps involved in the interrupt sequence of an 8086-8259 system. Also explain the initialization sequence of 8259 using a flow chart.	4	3	4	2
15. a)	Draw and discuss the architecture of 8257.	4	2	5	1
b)	Explain in brief the signal descriptions of 8251.	4	3	5	1
16. a)	Draw and explain in detail the flag register configuration of 8085.	4	2	1	1
b)	Draw and discuss the flag register configuration of 8086.	4	2	2	1
17.	Answer any two of the following:				
a)	Draw and discuss briefly the architecture of 8253 timer.	4	2	3	1
b)	Draw and discuss the status register of 8257.	4	3	4	2
c)	Explain the architecture of 8251.	4	2	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level - 1	20%
ii)	Blooms Taxonomy Level - 2	40%
iii)	Blooms Taxonomy Level - 3 & 4	40%
